PRACTICAL CHIP DESIGN

EDN Executive Editor Ron Wilson explores how IC design teams really work: the struggle for power efficiency and performance, wrestling with semiconductor processes and design methodologies, the challenges of global design teams. How do we somehow herd architecture, IP, design and verification into a successful tape-out?

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Monday, September 7, 2009

Consumers' appetite for video drives new telecom silicon

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Consumers in China and Japan share at least one preference with those in the US and Europe: no one wants to go to a video store or theater if they can download video at home. This fact is changing the nature of the telecommunications buildout in developing markets such as China and India, and it is forcing replacement of central-office and customer-premises hardware in countries that already have a complete telecom infrastructure.

The root cause of the problem is high-definition video. Existing DSL connections and many cable services just don't deliver the effective bandwidth to subscribers to handle on-demand HD. This is forcing telecoms carriers, who desperately want the video delivery revenue, to move from the DSL they barely have made work to VDSL or VDSL2 to get the bandwidth they need over their existing twisted pairs. Eventually,

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Ethernet Passive Optical Networks (EPONs) or Gigabit Passive Optical Networks (GPONs.) And it is causing new buildout in developing markets to be primarily FttH.

This global upgrade is a windfall for the semiconductor suppliers who have tied into the telecom market. The changes require new transceiver silicon to handle VDSL or optical links, as well as new aggregator and packet-management silicon to handle the high bit-rate packet streams as they come off the transceivers at the central office. The intense interest in this market is reflected in three announcements that all hit this morning.

The push to get more revenue from twisted pairs translates into the need to get nearly 100 Mbits/s over the median local loop, while using as little power as possible and providing essentially 100 percent up-time. To this end **Ikanos Communications** this morning announced a new line of Velocity chipsets: 8-port, 100 Mbit/s VDSL access devices that combine **DSP**, analog front ends, and driver-receiver chips into a six-chip set for 8 ports. The company claims under 1 W/port.

Intended for central-office application, the sets support a range of reliability and QoS features tuned for delivery of HD video over IP in a mixed stream with IP voice and data packets. Additional features extend the range of the transceivers at high bit rates for service over the longest and most problematic loops, and support survival of the connection during random and burst impulse hits and through line drops of up to a second. The company emphasized that not just throughput but robustness, in the experience of the carriers, was necessary for the customer to find the service acceptable, and that robustness started with the architecture and algorithms in the VDSL transceivers.

There's a similar push on the optical side. But here the issue is not the bit rate, but the cost. FttH connections are mostly provisioned with relatively expensive discrete optical parts that require mechanical assembly and alignment—fine for a demonstration service, but too expensive for a massive build-out in a developing market. In answer to the problem, this morning **OneChip Photonics** announced an office/subscriber pair of single-chip EPON transceivers. The chips use the 1490/1310 nm wavelength pair to achieve up to 2.5 Gbit/s in a single fiber. The company claims that its Indium Phosphide IC technology allows all active and passive transceiver components to be integrated into a single on-chip waveguide structure. The company fabricates this structure in a single epi growth, slashing manufacturing cost. OneChip also claims its laser and detector structures independently outperform competing Fabry-Perot lasers and avalanche photodiode detectors.

Once all that data gets to the line card, something has to switch it. That is the realm of the morning's third announcement, **Cortina Systems'** CS8222/8224 aggregation switches. The chips integrate a switch engine capable of handling what appears to be an industry-leading 128 subscriber lines, a packet-classification engine, a controlling 400 MHz ARM 11, the necessary MACs on the subscriber side and SerDes on the backplane side for connectivity, and a separate port for VoIP traffic, all on one die.

The 8222 aggregates DSL ports, and the 8224 handles Ethernet ports, generally from fiber transceivers. With on-chip packet inspection the Cortina chips support QoS strategies for mixed video/voice/data traffic, and can manage mixed services on

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with an upgrade path so that they can use the 8222 today to generate increased revenue from the existing copper plant with video services, and them move gradually, through line-card swaps, to optical FTTH service.

It appears that one of the interesting dynamics of this market will be the effort to deal with quality-of-service, services management, billing, and the many related things that all rest at their foundation on packet classification and scheduling. Whether these operations are done in the aggregating switch, in the transceivers, or deeper in the carrier's or service provider's network appears to be a bit up in the air. That is forcing silicon providers to work directly not only with systems vendors but also with carriers and cable companies in creating specifications for new chips. And this involvement, in turn, is transforming the surviving silicon vendors into systems architects, expected to provide virtually an entire network reference design to carriers before they can sell chips to the systems vendors. It's a rather upside-down supply chain, and it will be very interesting to see how stable it really is.

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at 9/8/2009 2:20:53 PM, webster said:

I think you meant "Cortina Systems", not "Contina".

fyi...

at 9/8/2009 4:23:48 PM, ron said:
webster:
right you are, thank you. I've corrected it.
ron

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